CLAIMS

1. A method for presenting an interlaced frame, said method comprising:

deinterlacing the interlaced frame, thereby resulting in a deinterlaced frame; and

scaling the deinterlaced frame.

2. The method of claim 1, further comprising:

decoding the interlaced frame.

3. The method of claim 2, wherein decoding the frame further comprises:

decompressing the frame, thereby resulting in the interlaced frame.

4. A system for presenting interlaced frames, said system comprising:

a video decoder for decoding interlaced frames;

a deinterlacer for deinterlacing the interlaced frames, thereby resulting in deinterlaced frames; and

a display engine for scaling the deinterlaced frames.

5. The system of claim 4, wherein the video decoder further comprises:

a decompression engine for decompressing the interlaced frames.

6. The system of claim 5, wherein the video decoder comprises:

an MPEG-2 video decoder for decompressing the interlaced frames.

7. A system for presenting interlaced frames, said system comprising:

a video decoder for decoding interlaced frames, the decoder further comprising a deinterlacer for deinterlacing the interlaced frames, thereby resulting in deinterlaced frames; and

a display engine for scaling the deinterlaced frames.

8. The system of claim 7 wherein the decoder further comprises:

a decompression engine for decompressing the interlaced frames.

9. A system for presenting interlaced frames, said system comprising:

a video decoder for decoding interlaced frames;

a display engine for scaling deinterlaced frames, wherein the display engine further comprises a deinterlacer for deinterlacing the interlaced frames, thereby resulting in the deinterlaced frames.

10. The system of claim 9, wherein the display engine further comprises a scaler for scaling the deinterlaced frames.

11. A circuit for presenting interlaced frames, said circuit comprising:

a processor; and

a memory connected to the processor, said memory storing a plurality of instructions executable by the processor, wherein execution of the plurality of instructions by the processor cause:

receiving interlaced frames;

deinterlacing the interlaced frames; and

scaling the deinterlaced frames.

12. The circuit of claim 11, wherein execution of the plurality of instructions by the processor further causes:

decoding the interlaced frames.

13. The circuit of claim 11, wherein execution of the plurality of instructions by the processor further causes:

decompressing the interlaced frames.

14. A decoder for decoding interlaced frames, said decoder comprising:

a decompression engine for decompressing the interlaced frames; and

a deinterlacer for deinterlacing the interlaced frames.

15. A display engine for scaling interlace frames, said display engine comprising:

a deinterlacer for deinterlacing the interlaced frames, thereby resulting in deinterlaced frames; and

a scaler for scaling the deinterlaced frames.